# EUTELSAT

**Organisation européenne de télécommunications par satellite**
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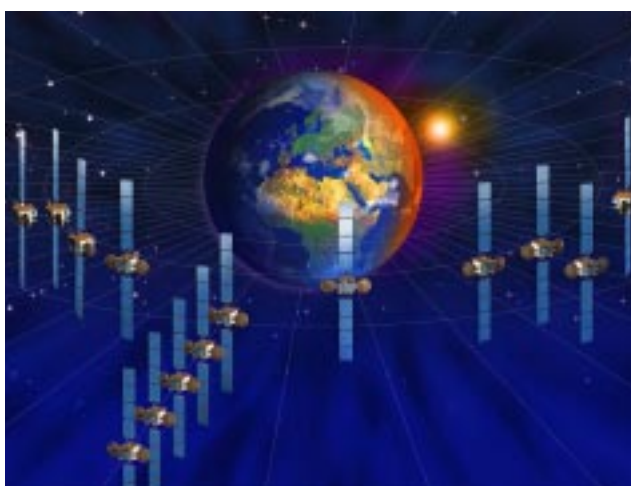70, rue Balard — 75502 PARIS Cedex 15 — France

DiSEqC 1.0

DiSEqC 2.0

Digital Satellite Equipment Control (DiSEqC™)

# SIMPLE "TONEBURST"

# DETECTION CIRCUIT

August 12, 1996

**Reference Documents that define the DiSEqC System:**

DiSEqC™ Bus Specification Version 4.2 (February 25, 1998)

DiSEqC™ Slave Microcontroller Specification Version 1.0 (February 25, 1998)

DiSEqC™ Logos and Their Conditions of Use (February 25, 1998)

**Associated Documents:**

Update and Recommendations for Implementation Version 2.1 (February 25, 1998)

Application Information for using a "PIC" Microcontroller in DiSEqC™ LNB and simple switcher Applications Version 1.0 (June 7, 1999)

Application Information for Tuner-Receiver/IRDs (April 12, 1996)

Application Information for LNBs and Switchers Version 2 (February 25, 1998)

Reset Circuits for the Slave Microcontroller (August 12, 1996)

Simple Tone Burst Detection Circuit (August 12, 1996)

Positioner Application Note Version 1.0 (March 15, 1998)

# CONTENTS

# 1.     Introduction

The DiSEqC Bus was designed primarily to control satellite peripheral accessories via the standard coaxial feed cable of Tuner-Receiver/IRDs in DTH and SMATV installations. It provides a comprehensive range of switching facilities and the capacity for many more sophisticated applications in the longer term.

A dedicated microcontroller (the "Slave") has been developed primarily to respond to the switching commands for various accessories. When several separate selection functions are required (e.g. polarisation, frequency band, and different satellite orbital locations) in a single module such as a LNB or SMATV Switcher, the microcontroller provides a very economical solution (especially as it also supports the established voltage and tone signalling methods). However, when only a simple two-position selection switch is required, it is difficult for a microcontroller to be competitive if low-cost is the only consideration. Therefore, a simple signalling method was devised which is compatible with the DiSEqC system, but which can control a two-position switch using simple hardware.

This document defines the "ToneBurst" control signal and describes a simple hardware design which can reliably decode it.

# 2.     Description of the ToneBurst

Like the DiSEqC system, the new control method had to be compatible with the existing voltage (13/18 volt) and continuous tone (22 kHz) signalling methods. It could have been either a "continuous" signalling method (like the voltage and tone systems), or a "command" method as with any normal control bus such as DiSEqC. The two methods have very different, and to some extent, complementary characteristics.

Apart from simplicity, an advantage of continuous signalling methods is that if a transient effect causes an error, then the decoding circuit can automatically recover, whereas an error in a command system must remain until a new "message" is sent. A disadvantage is that continuous signals may interfere with, or at least compromise, the performance of other continuous signals. It can be argued that the addition of the 22 kHz continuous signal itself reduced the tolerances on the 13/18 volt levels (because there does not appear to be any standardisation as to whether the tone is applied symmetrically on the supply voltage, or "sits up" or is pulled down). The addition of a further continuous tone, or modulation system, could introduce further interactions, particularly when it is noted that most "22 kHz tone" detectors are very simple with little or no frequency selectivity.

Thus a "command" method was selected as being most compatible with existing systems, and with DiSEqC itself. Only two commands are defined (corresponding to the two inputs of a two-way switch) which nominally select "Satellite A" and "Satellite B".

To provide software commonality with DiSEqC, one of the signalling commands was chosen to be a burst of 22 kHz tone modulated in the same way as a single DiSEqC data byte. The reason for using only a single byte (i.e. 9 cycles, including the parity bit, each nominally of 1½ easily from true DiSEqC command messages which have a duration of at least three bytes (i.e. about 40 ms). This "ToneBurst" command is defined as a sequence of '1' data-bits, which have a nominal modulation of 1 : 2 mark : space ratio, and thus average to 1/3 of the unmodulated carrier level.

The second signalling command could have been a DiSEqC data-byte containing entirely '0' data-bits, but this modulation averages to 2/3 of the unmodulated carrier level which is not easy to discriminate from the 1/3 level with simple, cheap hardware. Therefore, the second command was chosen to be an unmodulated toneburst, with the same duration as the first, i.e. nominally 12½ ms can be discriminated either by detecting the difference in their average carrier levels, or by detecting if the 1½ ms period bit-modulation is present.

'0' Tone Burst (Satellite A)

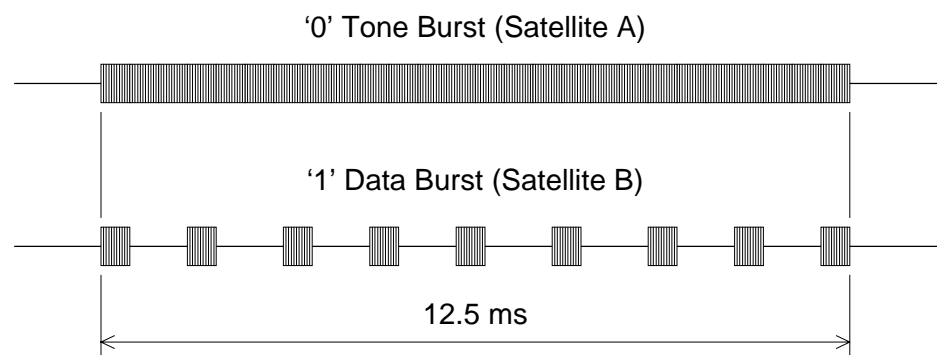'1' Data Burst (Satellite B)

12.5 ms

**Figure 1: ToneBurst Commands**

# 3.  Specification of the ToneBurst

Most characteristics of the ToneBurst follow on from the original definition of the 22 kHz tone signalling (e.g. IEC 1319-1) and from the DiSEqC Bus specification. The basic characteristics are thus:

| | | |
|---|---|---|
| Carrier frequency | = | 22 kHz ± 20% |
| Carrier amplitude | = | 650 mV peak-peak ± 250 mV |
| Modulation mark period | = | 500 µs ± 100 µs |
| Modulation space period | = | 1 ms ± 200 µs |
| ToneBurst duration | = | nominally 12½ ms[a] |

   a. It is expected that the ToneBurst normally will be generated in Tuner-Receiver/IRDs under microprocessor control, where the number of bit-periods can be accurately set. If simple hardware ToneBurst generators are constructed, it is recommended that the ToneBurst should be lengthened to ensure that the number of modulation cycles is never less than 9, even with adverse (non-tracking) tolerances.

In addition, it is necessary to provide a "code of practice" to ensure that very simple hardware can decode the ToneBurst when it is used in combination with the voltage and continuous tone signalling methods, as shown in *Figure 2*. The principle recommendation is that any DiSEqC message, change in the 13/18 volt signalling level, termination of a continuous tone, or any combination, must be followed by the relevant ToneBurst command. This is to ensure that a simple decoder, which may be disturbed by any of the above signals, is re-set to the correct state. However, the circuit presented later in this note should be immune to disturbance by any of these signals (except DiSEqC "Reply" messages).
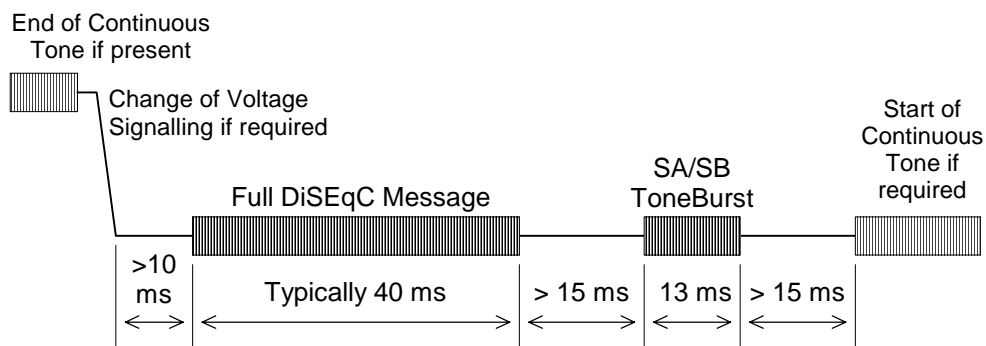


**Figure 2: Combined Tone, Voltage, DiSEqC and ToneBurst signalling**

# 4. Hardware Design Targets

The basic characteristics of the 22 kHz tone were described in *section 3.*, but to allow for voltage drop in the cable, and the fact that the signals are not truly sinusoidal, it is wise to assume a voltage range of at least 300 millivolts to 1 volt peak-peak. An even higher sensitivity may be of benefit in some cases, but it would be wise to ensure that the detector does not respond to signals of less than 100 millivolts at any frequency.

A nominal bus supply voltage of 15 volts d.c. has been assumed, which can then vary by up to ±3 volts for the H/V (polarisation) signalling, tolerances and voltage drops. The design tolerancing might be easier if the Vcc for the whole circuit (or just the bias networks) is stabilised at say 9 volts by a zener diode, but this could limit the usefulness of the switching (flip-flop) output stage, and represents an added cost. Therefore, the Vcc for the whole circuit is assumed to be fed directly from the bus, with perhaps just a small decoupling capacitor (of say 100 nF).

For the simplest applications, it does not matter if the switch is disturbed by DiSEqC commands, by H/V voltage-switching steps, or at the end of a continuous tone, because the protocol demands that a valid ToneBurst is always transmitted shortly afterwards. However, it is better to avoid unnecessary switching, and interruption of the path must be avoided if true DiSEqC commands (or power) are being passed through the switch to other (Slave microcontroller) accessories.

The design presented here is therefore resistant to voltage-steps and includes a time-gate so that it is not activated by tone-bursts of more than about 25 ms, i.e. full DiSEqC Command messages (3 bytes) and the end of a continuous 22 kHz tone. In two-way DiSEqC systems it may be affected by the (1 and 2 byte) "replies" until the master re-sends the correct ToneBurst status (a few tens of milliseconds later). If it is important for the switch not to be disturbed by these replies, then an additional delay network of say 50 ms (before the final output switches over) could be added.

The aim was to make the circuit as simple as possible, but to be capable of being produced reliably in production quantities. A further target was to use a single, standard integrated circuit with peripheral components of moderate accuracy and value. Generally, resistors of ±5 % and capacitors of ±20 % tolerance, and availability of values of up to 1 MΩ and 100 nF, were assumed, which should be realistic for conventional (through-hole) printed circuit construction. These limit values and tolerances may not be as readily available in sub-miniature and Surface Mounting form, so it may be necessary to adapt the design to suit the specific limitations of these components. However, it is only practical to fully optimise a design when all the price and performance, etc. parameters are known.

The LM324 op-amp integrated circuit chosen presents some design difficulties because, although being of a long-established type, a few of the limit parameters are not given in the manufacturers' data. Input offset voltages are negligible in this application, and the effects of input current variation are controlled by avoiding excessively high resistance values. However, some frequency-dependent parameters are neither fully-specified, nor negligible. Ideally, an op-amp should be operated with sufficient feedback to swamp variations in the device's characteristics, but, like many cheap internally-compensated op-amps, the voltage gain of the LM324 falls when moving up from quite low frequencies, and is only moderate at the required 22 kHz. It is recommended to verify satisfactory operation with a number of I.C. samples, preferably from different sources and manufacturers, or at least ensure that components which are purchased for production are obtained from the same vendor as used for the initial validation.

# 5. Circuit Description

*Figure 3* shows a basic block diagram of the ToneBurst Decoder, where the bold-line boxes represent active (op-amp) stages, and the remaining boxes are passive circuits. It uses the principle of specifically detecting the presence of amplitude modulation on the ToneBurst, rather than simply comparing the average level of the burst with the (peak) carrier level. Although it is possible to detect a nominal ratio of 1 : 3 in the average (low-pass filtered) levels of modulated and unmodulated bursts respectively, it became apparent that simple level-detection circuits were difficult to apply when time-constant deviations of more than about 20 % (primarily capacitor tolerances) might occur.
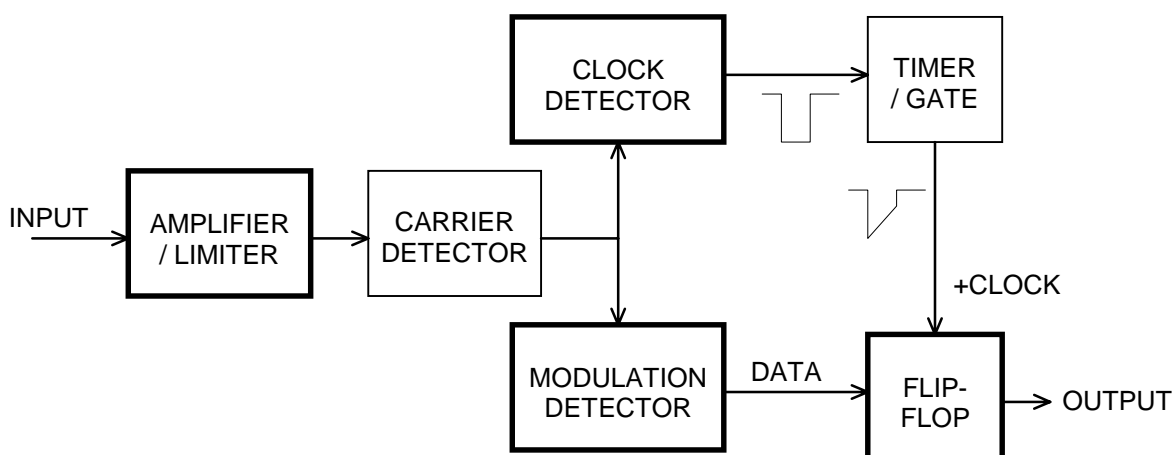


**Figure 3: Block Diagram of the ToneBurst Decoder**

The Amplifier/Limiter stage increases the 22 kHz tone amplitude to a level which can be detected by a simple diode Carrier Detector. The Clock Detector employs a low-pass filter and level-detector to determine the start and end of each Toneburst (irrespective of whether it is modulated or not). It produces a negative-going pulse (from Vcc to earth) during the ToneBurst. This drives the passive Timer / Gate which feeds the trailing (positive) edge of the clock pulse onto the output flip-flop only if it occurs within about 25 ms of the leading edge. The Modulation Detector includes another level-detector which monitors the voltage generated by a modulation "pump" circuit. It thus determines whether the ToneBurst is modulated or unmodulated, and provides an output of 0 volts or Vcc respectively. The output Flip-Flop stage receives both this 'Data' signal and the gated clock signal, it copies the state of a 'valid' ToneBurst and drives a relay or an electronic (diode) switch.

# 6.  Detailed Circuit Description and Design Details

The complete circuit is shown in *Figure 4*, and is designed around four operational-amplifiers in a single package, with ancillary gating functions performed by diodes. The well-established LM 324 is used because it can operate in a single supply-rail configuration with inputs biased as low as earth (0 volts), and its outputs can drive almost fully between the rails (at low current). The diagram also includes a few optional "refinements" which may help with the operational tolerances, but add to the complexity. Therefore, these refinements are drawn with thin lines and are described in *italics*.

The bistable (flip-flop) output stage does require a significant number of peripheral components, but it has the advantage (compared with an HCMOS flip-flop) that it uses a "spare" op-amp in the i.c. package and does not need a separate (regulated) supply rail. Also, it can give a large output voltage swing (almost 0 volts to Vcc at low current), and can deliver sufficient current for a relay.
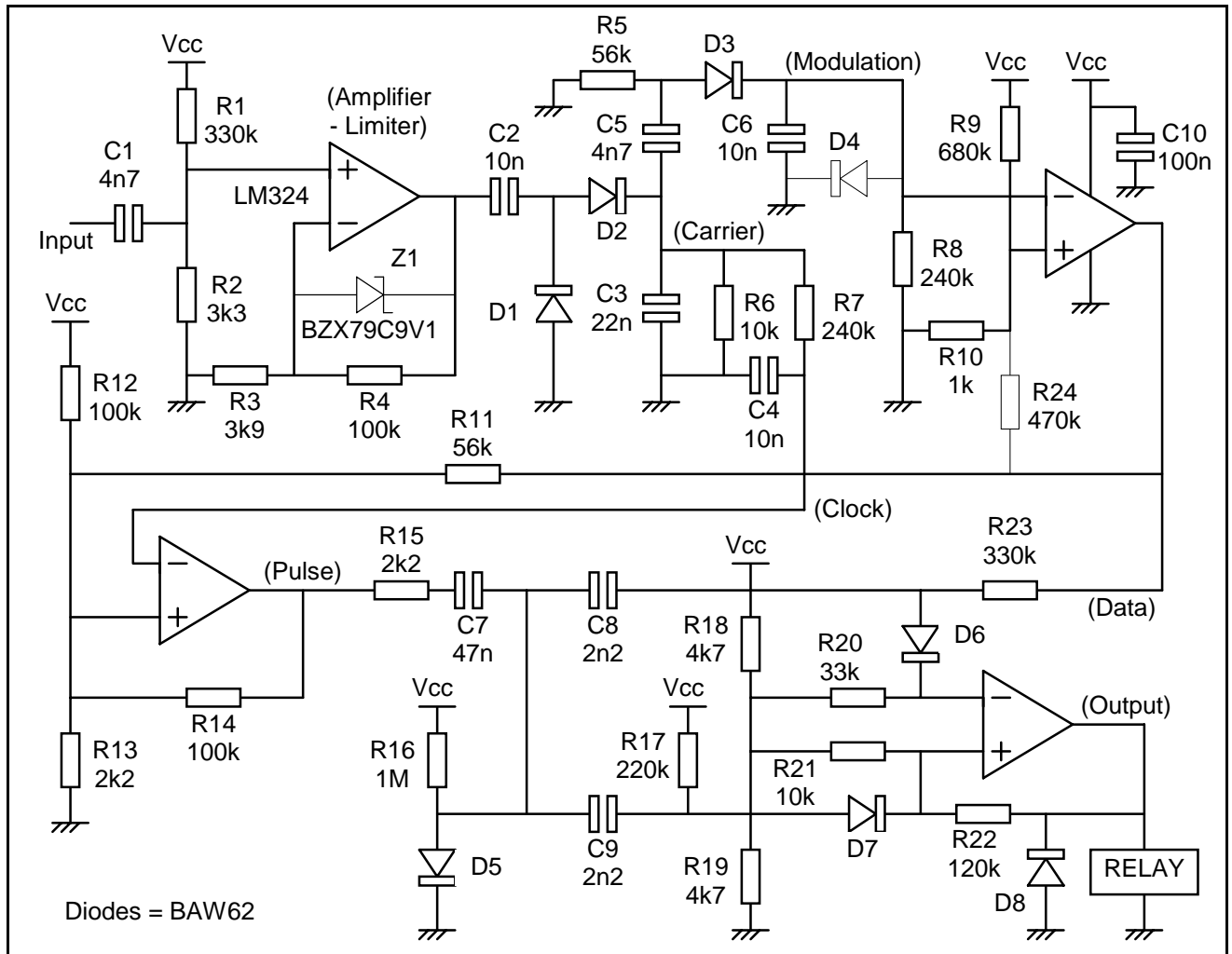


**Figure 4: Circuit Diagram of the ToneBurst Decoder**

The method of operation, and the basic design considerations are as follows:

# 6.1.  Amplifier/Limiter

The minimum 22 kHz input level (from the Bus) may be about 300 millivolts pk-pk (allowing for some drop in the cable), and the maximum about 1 volt pk-pk. Although the detector circuits can tolerate some variation of signal amplitude, a ratio of more than 1 : 3 could produce difficulties, so some form of limiting is of benefit.

The LM324 has a typical output slew-rate of 300 millivolts per µm, so the maximum "undistorted" sine-wave amplitude at 22 kHz can be about 4 volts pk-pk and the maximum triangular wave about 6 volts pk-pk. Operating the amplifier only in its "linear" mode would mean the minimum signal amplitude might be only about 1 volt pk-pk which would be difficult to detect (with diode forward voltage drops of up to 0.7 volt).

The simplest solution seems to be to operate the amplifier mainly in slew-rate limiting, i.e. with a "triangular" output of typically 6 volts pk-pk. Although the amplitude may vary by ±20% with the frequency, and an undefined amount with i.c. tolerances, this should be better than the initial voltage ratio of more than 1 : 3.

Thus the feedback resistors on the input amplifier are set to give a voltage gain of about 25 [ gain = (R3+R4) / R3 ]. This mainly sets the d.c. conditions because the small-signal gain of the LM324 at 22 kHz is not much greater than 20 anyway. The input bias is set to nominally 0.15 volt [ bias = Vcc x R2 / (R1+R2) ] to give a d.c. output level of about 4 volts [ bias x gain ].

Even with an optimally small input capacitor, C1 (4.7 nF has a reactance of about 1.5 kΩ at 22 kHz), a 5 volt step at the input pushes the amplifier output near to Vcc for a significant time, and if directly coupled would overload the simple diode detector, causing false-triggering. Therefore, the amplifier output is coupled by an optimally-small capacitor, C2, to block most of the energy associated with d.c. voltage transitions.

If the 13/18 volt level is changed with a mechanical switch (or a relay), there is the risk that "contact bounce" will produce more than one voltage edge. If the bounce is too severe it may simulate the 22 kHz tone and produce an error. *This effect can be reduced with the optional zener diode, Z1, on the input amplifier, which limits each "pump" cycle to about 8 volts swing rather than the unlimited 15 volts.*

*However, the zener diode produces fixed limiting at about +9 volts whereas the basic d.c. output bias voltage "tracks" up with increasing Vcc. Thus there is the risk that an increasing Vcc will actually <u>reduce</u> the peak-peak output voltage. This is one reason why the limiting zener is chosen as high as 9 volts (also, lower voltage zener diodes tend to have a poorly-defined "soft" knee at low currents). A possible solution is to regulate the input bias voltage chain, for example by using a forward-biased diode or a zener diode.*

*A useful substitute for the zener diodes above can be the reverse base-emitter junction of a small-signal silicon planar transistor. Although the breakdown does not have a tightly-specified voltage it is typically in the range 6 - 8 volts and has an exceptionally sharp knee (down to a few µA).*

## 6.2. Carrier detector

The carrier detector (D1, D2, C3 and R6) operates as a peak-peak ("voltage-doubler") "pump" circuit with a low resistance value (R6) as the dominant load on the network. It has a short (decay) time-constant of about 200 µs [ **t**c = C3 x R6 ] so that the voltage falls rapidly towards zero when there is no 22 kHz carrier.

## 6.3. Modulation (Data) Detector

The modulation detector (R5, C5, D3 and C6) detects the undulating voltage across the carrier detector. It could be another peak-peak detector, like the carrier detector, but the resistor (R5) which replenishes charge in the coupling capacitor (C5) should be cheaper and seems to give better performance than a diode. In particular it seems less liable to be affected by a small amount of residual carrier-ripple (22 kHz) from the carrier-detector. The optimum resistance for R5 is not easy to calculate, but the value is not critical, and a simple trial to obtain approximately the maximum detected amplitude seems adequate.

The modulation detector does not behave exactly as might be expected because a significant voltage rise is introduced onto C6 by the leading edge of the ToneBurst, <u>whether it is modulated or not</u>. The magnitude of this voltage is not easy to predict, but is typically up to about 1 volt. Optimum system operation seems to be obtained with C5 being about half the capacitance of C6.

If the ToneBurst is <u>not</u> modulated then the initial voltage step decays away exponentially during the burst. However, if the ToneBurst is modulated then the voltage on C6 is pumped back up to about the initial level by each cycle of the modulation. Thus at the end of the ToneBurst, the voltage on C6 is significantly higher if the burst was modulated than if it was not modulated.

Although there is potentially a large proportional difference in the voltages produced by the modulated and unmodulated ToneBursts, there are several factors which degrade the detection mechanism. Firstly, the amplitude of the ToneBurst is variable, and the diode forward-voltage drops and the cascading of the detectors magnifies these variations. Secondly, as shown in *section 6.4.*, detection of the end of the ToneBurst may be delayed by up to 5 ms, whilst the detected voltage decays at a rate which depends on component tolerances.

*Table 1* lists how the percentage voltages to and from a "final" aiming voltage vary exponentially on a simple R-C network, at times normalised to various multiples of the time-constant. This allows simple estimation of residual voltages to be made in the following calculations without the need to present or solve complex equations.

A nominal decay time-constant of about 2½ ms [C6 x R8] was chosen for the modulation detector, so that a period of at least 5 times the time-constant elapses before the end of the ToneBurst is reached. For this case, *Table 1* shows that the voltage decays to less than 1 % of the initial value, so an initial step of 1 volt should become less than 10 millivolts when the end of an unmodulated ToneBurst is detected. Conversely, a minimum detected voltage (of say 300 millivolts) at the end of a modulated ToneBurst may decay by up to 2½ time-constants, i.e. down to about 10 % (or 30 millivolts) before the end of the ToneBurst is actually detected. Thus the optimum "decision" level for detecting the presence of modulation is about 20 millivolts [ set by Vcc x R10 / (R9 + R10) ]. *If a more adverse variation of detected amplitudes is anticipated, then the maximum voltage which appears across C6 can be limited to about 700 millivolts by the addition of the optional diode, D4.*

*A further option is to introduce positive feedback (via R24) around the comparator to ensure that it switches rapidly between the two output Data levels. However this resistor does not significantly affect the actual data "decision" process.*

| Normalised elapsed time (Time-constants) | Percentage of final voltage reached | Percentage of final voltage remaining |
|:---:|:---:|:---:|
| 0.1 | 10% | 90% |
| 0.2 | 18% | 82% |
| 0.3 | 26% | 74% |
| 0.4 | 33% | 67% |
| 0.5 | 39% | 61% |
| 0.7 | 50% | 50% |
| 1.0 | 63% | 37% |
| 1.5 | 78% | 22% |
| 2.0 | 86% | 14% |
| 3.0 | 95% | 5% |
| 4.0 | 98% | 2% |
| 5.0 | > 99% | < 1% |

**Table 1: Exponential Charge/Discharge Characteristics**

## 6.4. "Clock" detector

The "clock-pulse" detection signal is obtained by low-pass filtering the carrier-detector signal with a simple time-constant of about 2½ ms [$t$a = C4 x R7]. This gives an "attack" delay to prevent false-triggering by disturbances such as the H/V signalling voltage steps and removes some of the data-bit ripple (1.5 ms period). The op-amp compares this signal with a voltage threshold defined across R13 and produces a negative-going pulse (i.e. from Vcc to earth) when the threshold is reached. Positive feedback is applied around the comparator (via R17) to give rapid switching, and to give sufficient hysteresis to prevent the clock output "dithering" due to modulation ripple on C4.

Again using *Table 1*, for a nominal 1 ms gap in the carrier (i.e. a '1' data bit), the voltage on C4 with a 2½ ms discharge time-constant "sag" by about 33 %, i.e. the peak-peak ripple is about 33% of the (present) peak voltage. In the worst case, a maximum gap (1.2 ms) combined with a minimum time-constant [ -25% = 1.9 ms ] could have a ripple of nearly 50 % (but should be somewhat less because of the finite fall-time of the signal on the carrier-detector). Thus a nominal positive feedback hysteresis of 50% of the detection level seems appropriate. Since the clock output swings almost from Vcc to 0 volts, this implies that R12 and R14 (which are each initially feeding current from Vcc into R13) should be of similar value.

The clock-pulse must be detected reliably and not later than, say, the second modulation cycle, i.e. after no more than 1 ms of carrier duration. With a worst-case time-constant [ +25 % = 3.2 ms ] this corresponds to about 0.3 of the time-constant, or about 25 % of the final "aiming" voltage.

It is difficult to calculate the exact aiming voltage, because of the complex voltage drops in the detector circuit, due to the coupling capacitor and op-amp source impedances, and the narrow conduction angle of the diodes with a triangular waveform. However, with a 6 volt peak-peak waveform it is reasonable to assume at least 3 volts on C3. Thus the clock detection level should be about 25 % of this, or 750 millivolts.

Assuming a value of 2.2 kΩ for R13 and a maximum Vcc of 18 volts, then a total resistance of [ 2.2 x 17.25 / 0.75 ] or about 50 kΩ to Vcc is required. Since the clock output is initially close to Vcc, and R12 and R14 should be about equal (for the hysteresis), they each can be nominally 100 kΩ.

Once the clock is triggered, the hysteresis lowers the restoration threshold to about 0.4 volt, but the detector voltage (across C4) may rise as high as 4 volts at the end of an unmodulated ToneBurst. Thus the voltage may have to decay by about 90 % (back to 0 volts) before the clock pulse terminates. This could take about 2½ time-constants, or 8 ms in the worst case, which is too long for the correct Data (modulation) level to remain detectable at the Data-comparator input.

Therefore, R11 is added which raises the threshold voltage (across R13) when the Data line is high (i.e. if the ToneBurst is not modulated), and makes the clock-pulse terminate earlier. This does not affect the timing or detection of the leading edge of the clock-pulse, because the Data line is always low just after the start of a ToneBurst (due to the voltage step produced on the modulation detector at the leading edge of every ToneBurst). Since the clock detector voltage is about 3 times higher at the end of an unmodulated burst compared with a modulated burst, the clock comparator level is raised similarly, i.e. by making R11 about half of the value of R12. This gives similar clock turn-off delays after modulated and unmodulated ToneBursts, with a maximum delay of about 1½ time-constants, or less than 5 ms.

## 6.5. "Time-out" gate

The "time-out" gate is predominantly C7, D5 and R16. When the clock pulse falls from Vcc to ground, the anode of D5 is pushed down to nearly minus Vcc, and then rises exponentially towards Vcc. After a period of about 0.7 time-constants [ C7 x R16 ] the voltage becomes positive and D5 conducts. If the positive edge of the clock pulse occurs before this time then a positive edge is applied to the bistable (flip-flop) stage (via C8, D6 and/or C9, D7). However, if the edge occurs later, then no triggering can occur because the forward-conducting diode causes virtually all of the voltage swing from the op-amp to appear across R15. Since the "gate" must be open for longer than the ToneBurst (say 25 ms), a time-constant [ C7 x R16 ] of about 40 ms is required.

*If the timing capacitor value is considered inconveniently large, then it is possible to use a lower "aiming" voltage for the exponential voltage rise. If the hardware already includes a lower voltage reference (e.g. zener or forward diode), then this may be suitable. Alternatively, it is possible to aim for the earth rail (0 volts), although the tolerancing is rather more difficult:*

*If the final aiming voltage is 0 volts, then even after a long timing period there still must be a voltage step of at least one diode forward-drop, although the flip-flop is not required to be triggered. By increasing the amount of hysteresis in the flip-flop (section 6.6.) it should be possible to ensure that the flip-flop is not triggered by voltage steps of less than 1.5 Volts, say. Then, the gate would effectively close when the exponential voltage reaches about -0.8 volts (i.e. 1.5 Volts minus the diode forward drop). This represents about 5 % of the starting voltage and occurs after about 3 times the time-constant. Thus the capacitor, C7, could be about 5 times smaller if the same-valued timing resistor, R16, was taken to earth rather than to Vcc. However, to give predictable timing, C7 needs to be significantly larger than the pulse capacitors (C8 and C9), so some reduction in the timing resistor (R16) may be appropriate.*

## 6.6. Output "Flip-Flop"

The bistable (flip-flop) function is implemented by applying positive feedback around another op-amp, with positive trigger pulses applied to the two amplifier inputs. The two op-amp inputs are biased at about ½ Vcc (via R20 and R21 from the divider chain R18 and R19) to suitably bias the steering diodes (D6 and D7), and so that the positive feedback (via R22) gives symmetrical hysteresis. The hysteresis must be at least sufficient to prevent the flip-flop being toggled directly by the bias currents through R17 and R23. *It will need to be larger if the short time-constant gate circuit described in 6.5 is used.*

With the "pulse-plus-bias" gates (C8 + D6 + R23 and C9 + D7 + R17), the clock-pulse negative edge has no effect on the flip-flop because it simply reverse-biases the steering diodes. If there is a sufficiently large positive clock edge (greater than about 1 volt), then a brief positive pulse is applied to the op-amp positive input via D7. If the Data level is "low" (0 volts) then D6 is reverse-biased and the flip-flop latches with its output positive (i.e. close to Vcc). However, if the Data level is "high" (Vcc) then a positive pulse is also applied to the negative input of the op-amp. The 'Data' time-constant [ C8 x R20 ] is made significantly longer than the '1' time-constant [ C9 x R21 ] so that the pulse on the negative input remains effective longer than that on the positive input, and thus the flip-flop latches with its output low (i.e. close to 0 volts).

Because of time delays in the op-amp, the input pulses need to be some tens of micro-seconds long, which sets a minimum value for the pulse-capacitors (C8 and C9). The gate-bias resistors (R23 and R17) must have a sufficiently high resistance value that they cannot deliver enough current to toggle the flip-flop directly. However, the 'Data' bias resistor (R23) must give a sufficiently short time-constant with its pulse-capacitor (C8) to ensure that the bias voltage has stabilised (after a Data-level change) before the positive clock edge occurs. Rather like the "timeout" gate, this gate responds in about 0.7 of the time-constant [ C8 x R23 ], so with the values shown it may not be reliable to apply a trigger (clock pulse) positive edge within about 1 ms after a change in the Data level. In practice this is unlikely to occur because of the inherent delay in the end-of-ToneBurst detection mechanism.

A further limitation on the values of C8 and C9 is that if they are made too large (or if the flip-flop hysteresis is made too small) there is a tendency for the flip-flop to be directly triggered by steps in the supply voltage. A good compromise seems to be 2.2 nF, since the flip-flop typically triggers with capacitors of half this value.

D8 is the normal protection diode which is required across any inductive load such as the relay. The relay could be connected to Vcc instead of earth if the opposite operation polarity was required. Alternatively, the output can drive an electronic (diode) switch, if preferred.