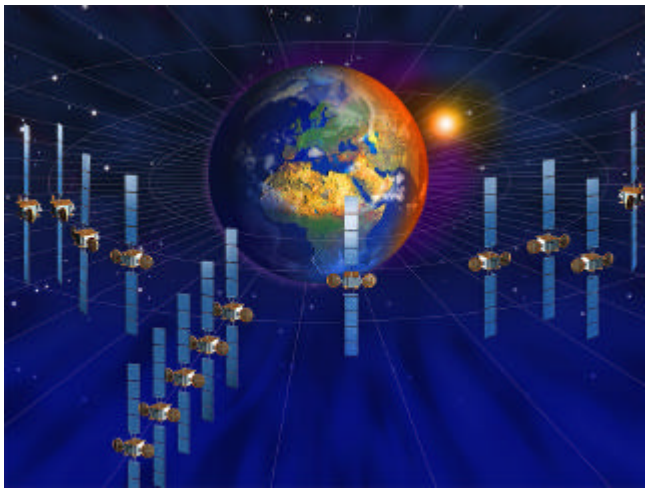
Organisation européenne de télécommunications par satellite
European Telecommunications Satellite Organization
70, rue Balard — 75502 PARIS Cedex 15 — France

Digital Satellite Equipment Control (DiSEqC™)



SLAVE MICROCONTROLLER

VERSION 1.0

February 25, 1998

Reference Documents that define the DiSEqC System:

DiSEqC™ Bus Specification Version 4.2 (February 25, 1998)

DiSEqC™ Slave Microcontroller Specification Version 1.0 (February 25, 1998)

DiSEqC™ Logos and Their Conditions of Use (February 25, 1998)

Associated Documents:

Update and Recommendations for Implementation Version 2.1 (February 25, 1998)

Application Information for Tuner-Receiver/IRDs (April 12, 1996)

Application Information for LNBs and Switchers Version 2 (February 25, 1998)

Reset Circuits for the Slave Microcontroller (August 12, 1996)

Simple Tone Burst Detection Circuit (August 12, 1996)

Positioner Application Note Version 1.0 (March 15, 1998)

CONTENTS

0. Status

This specification is a reformatted and slightly amended version of the "Slave Microcontroller Version 1.0" document dated April 18, 1997. Amendments are marked with vertical revision bars, but the only significant correction is to *Table 6*, which is now in accordance with *Table 2* of "Application Information for LNBs and Switchers", dated April 12, 1996. The microcontroller is now identified as Version 1.0, to reflect its mask-programmed status, but the program code is identical to the original Version 0.2 software.

1. Introduction

This document describes the Operational Functions of the Digital Satellite Equipment Control (DiSEqC™) Slave Microcontroller, version 1.0. Details of the DiSEqC™ Bus are in the DiSEqC™ *Bus Functional Specification Version 4.2* published by Eutelsat.

The DiSEqC™ Slave is a pre-programmed microcontroller dedicated to the reception of DiSEqC™ Bus commands for the control of peripheral accessories in DBS/DTH (Direct Broadcasting by Satellite / Direct To Home) systems. The microcontroller employed is a low-cost, single-chip version from the well-established 80C51 series. The standard version of the software is able to support most Slave applications by adapting itself to its hardware environment. This is performed in two ways; firstly, any dedicated output pin which is linked to ground indicates that the associated facility is not available. Secondly, a small array of diodes between appropriate "Strobe" and "Selection" pins indicates the characteristics of the external circuitry (e.g. LNB Local Oscillator frequency).

2. Device Characteristics

The microcontroller is a programmed version of the Philips Semiconductors' 8xC750 series of 80C51 derivatives, so full mechanical and electrical data may be found in the relevant data sheets. Development (and maybe custom OEM) versions are OTP (One Time Programmable) 87C748, 87C750 or 87C751 types, and the production version is mask-programmed in a 1 kbyte ROM implementation (83C750). First production is in a square 28 pin PLCC (Plastic Leadless Chip Carrier) package, but OTP samples can be in a 24 pin "skinny DIP" (0.3 inch row spacing Dual In- line Package), a small 24 lead surface mount (SSOP) package, or the PLCC package. All packages have the same pin sequence, but not the same pin numbering (the PLCC has 4 pins not connected). Generally, unless otherwise indicated, the pin numbers given in this specification (and in the circuit diagrams) refer to the DIL/SSOP packages.

2.1. Electrical Characteristics (dc)

The specified power supply voltage (Vcc) is 5.0 volts ± 10%.

At a nominal oscillator frequency of 6 MHz the typical current consumption of the chip is 6 mA.

The normal port pins in the 80C51 series of microcontrollers have "quasi bi-directional" characteristics. To achieve this, the on-chip circuitry provides a weak pull-up (source) current of about 50 µA, and a rather stronger pull-down (sink) current of a few mA when a logical '0' is written to the port pin. At power-up and reset, the microcontroller's internal hardware automatically sets all the port pins high. To use any pin as an input, the software leaves (or sets) the pin "high" and then the external signal only needs to sustain the relatively small pull-up current. When used as an output, an "active low" (sink) current of up to a few mA is available, or some "active high" (source) current may be obtained via an externally connected resistor of typically 3.3 kΩ to Vcc.

The switching characteristics for the normal port pins are:

Input "low" voltage	=	0.8 volts maximum at 4.5 volts Vcc
Input "high" voltage	=	2.0 volts minimum at 5.5 volts Vcc
Output "low" voltage	=	0.45 volts maximum at 1.6 mA (sink)
Output "high" voltage	=	2.4 volts minimum at 60 µs (source)

Three “Port 0” pins have an enhanced current sink capacity of 3.2 mA at a 0.45 volts “low” output, but no active pull-up circuitry. These pins are used to provide the “Standby” power control and the two configuration “Strobe” pulse outputs.

In the DiSEqC™ Slave application, most of the port pins are allocated to output functions, but are also used as inputs to determine whether each output function is actually required. At initialisation, the internal software allows each pin to float high, and it is tested to determine whether the pin actually is high. If not, the pin is assumed to be linked to ground and thus unused in the specific application. This places slight restrictions on the external driven circuit, for example direct connection to the base of a common-emitter driver stage is not permitted. This is because the base saturation voltage of about 0.7 volts would be detected as a “low”, i.e. the same as a hard-wired grounding link (implying that the output signal is not in use).

2.2. Active Characteristics

Version 1.0 internal software generates each cycle of the reply 22 kHz tone by dividing the clock oscillator by 288 (24 machine cycles). The oscillator frequency for generating an exact 22 kHz carrier is therefore 6.336 MHz, but a cheap 6 MHz crystal or ceramic resonator provides a frequency (20.83 kHz) which is well within the tolerances of the Bus specification (22 kHz ± 20 %). The external oscillator components can be the normal “π“configuration using a crystal (or 2-terminal ceramic resonator) and two 22pF capacitors, or a single 3-terminal ceramic resonator.

The reset circuitry incorporates a low-current internal sink, so just a single capacitor from the Reset pin to Vcc may be sufficient. However, some DiSEqC™ applications (where the Slave is powered via the Bus cable) require a moderately rapid but well-defined reset time (less than 100 ms), so the addition of a resistor of typically 22 kΩ from the Reset pin to Vss is recommended.

With the recommended clock frequency, the software tone-decoding (carrier-modulation detection) accommodates the expected variations of transmit frequency (22 kHz ± 20 %) and bit-period (1.5 ms ± 20 %).

3. DiSEqCä Slave Pin Names

Five pins are totally defined by normal 8xC75x hardware requirements. These are:

Vcc : The Power Supply rail of 5 volts ± 10 %

Vss : The system "Ground" or "Earth" potential.

Reset : Must be driven active high until the oscillator is fully operational.

X1, X2 : Oscillator using a 3-terminal ceramic resonator (or 2-terminal + 2 capacitors)

The remaining 19 pins have been allocated general circuit names (*Table 1*, and *Figure 2* in *section 9.*), and also DiSEqC™ family-specific input and output names as follows. Note that some of the family-specific functions are mutually exclusive, so not all can be used in any single application, nor are all implemented in the first versions of the DiSEqC™ Slave software.

Hi / Lo	: LNB local oscillator High and Low frequency selection [I/O]
H / V	: Horizontal / Vertical Polarisation selection [I/O]
SB / SA	: Satellite Position selection (A = the more-easterly when practicable) [I/O]
SW0 B/A	: "Options" Switch (e.g. B = Satellites 3 & 4, or Circular Polarisation) [I/O]
SW1 - SW4	: General Purpose (Uncommitted) Switches [I/O]
OP 1 - 8	: Decoded Outputs (1 of 8) for individual source switching
DTX	: DiSEqC™ Bus Transmit signal [Out]
DRX	: DiSEqC™ Bus Receive signal [In]
Standby	: Power-down the peripheral hardware [Out]
Volts (IPX)	: Signalling of 13/18 volts bus level, or local power supply status [In]
S0 - S3	: Data inputs to receive peripheral hardware configuration [In]
Strobe D, E	: Active-low pulses to signal data into S0 - S3 via diode array [Out]
B0 - B7	: Binary I/O pins for Installation Aids or D/A converter, etc. [I/O]
OPX	: General-purpose digital output, originally intended for PWM analogue output, but not supported in Version 1.0 software. [Out]
I/O	: General purpose inputs and/or outputs for use as required [I/O]

4. DiSEqCä Slave Microcontroller Pin Allocations

DIL pin number	PLCC pin number	8xC750 pin name	General circuit name	A (LNB or Switcher)	B (Comple-mentary Outputs)	C (Polariser)	D (Install-ation aid)
1	1	P3.4	OP 5	SW1	*Lo / Hi*	B4	B4
2	2	P3.3	OP 4	SW0	SW0 B/A	B3	B3
3	3	P3.2	OP 3	SB/SA	SB / SA	B2	B2
4	4	P3.1	OP 2	H / V	H / V	B1	B1
5	6	P3.0	OP 1	Hi / Lo	Hi / Lo	B0	B0
6	7	P0.2	SBY	Standby	Standby	Standby	I/O
7	8	P0.1	STR E	Strobe E	Strobe E	Strobe E	Strobe E
8	9	P0.0	STR D	Strobe D	Strobe D	Strobe D	Strobe D
9	11	Reset	RESET	Reset	Reset	Reset	Reset
10	12	Xtal-2	X 2	Xtal-2	Xtal-2	Xtal-2	Xtal-2
11	13	Xtal-1	X 1	Xtal-1	Xtal-1	Xtal-1	Xtal-1
12	14	Vss	Vss	GND	GND	GND	GND
13	15	P1.0	S 0	S0	S0	S0	S0
14	16	P1.1	S 1	S1	S1	S1	S1
15	17	P1.2	S 2	S2	S2	S2	S2
16	18	P1.3	S 3	S3	S3	S3	S3
17	19	P1.4	DTX	TX	TX	TX	TX
18	20	P1.5 (I0)	DRX	RX	RX	RX	RX
19	23	P1.6 (I1)	IPX	Volts	*Volts*	Volts	I/O
20	24	P1.7(T0)	OPX	*I/O*	*OPX*	*SW 0*	*SW 0*
21	25	P3.7	OP 8	SW 4	*SW 0*	B7	B7
22	26	P3.6	OP 7	SW3	*SA / SB*	B6	B6
23	27	P3.5	OP 6	SW2	*V / H*	B5	B5
24	28	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc

Table 1: DiSEqC Slave Microcontroller Pin Allocations

Some of the pins of the DiSEqC™ Slave IC have fixed functions, but other pins perform different functions depending on the application (family) to which the device is being put. Table 1 lists all the pins which have been allocated for four family types (A, B, C and D). DiSEqC™ Slave software version 1.0 is primarily concerned with family A with some support for the other families. The operational characteristics described in the remainder of this specification generally apply to family A (LNBs and Switchers) except where otherwise stated. Note that pin and control functions shown in italics are specific to the version 1.0 microcontroller software and may not be retained in future versions.

5. Definition of the Slave configuration

The Slave microcontroller software must determine from the external circuitry which functions are actually implemented, and for what purpose the multi-function pins are to be used. This is done at initialisation by scanning the voltage levels on various pins, both statically, and when each Strobe pin is activated. The various conditions which are tested for by the software are defined in the following subsections.

5.1. ‘Standby’, ‘Transmit’ and ‘OPX’ outputs

If the slave external hardware does not implement the ‘Standby’ or ‘Transmit’ functions, then the relevant output pins should be linked to earth (Vss). Thus, if circuitry is not included to remove power from the peripheral hardware (the DiSEqC™ chip and Bus-interface should always remain powered), then the Standby pin should be grounded.

Version 1.0 software does not test the “DiSEqC™ Transmit” (DTX) pin to determine whether it is possible to send a reply, since little use can be made of the information. The omission of this test may permit slight simplification of the transmit circuitry because it is not necessary to ensure that the output pin is able to rise above the minimum ‘1’ voltage level.

The ‘OPX’ output gives various alternative outputs (see section 7.6), depending on the “family”, as defined in section 5.5. In general the ‘OPX’ pin should be grounded unless the output function is actually being used.

5.2. Switching control lines

If any of the "Committed" or "Uncommitted" switching control lines are not relevant to the application (e.g. the "Options" switch, SW 0, and the Uncommitted switches, SW 1 - SW 4, in a normal LNB) then the associated control pins should be grounded. Also, any Committed functions which are fixed at the defined "default" states (i.e. Low Local Oscillator frequency, Vertical Polarisation, "Satellite position A" and "SW 0 position A") should be linked to ground. Any fixed function which is not consistent with these default states (i.e. High L.O. frequency, Horizontal Polarisation, "Satellite position B" and "SW 0 position B") should be connected via a signal diode to the "Strobe_E" pin (with cathode to the strobe).

Where practicable, "Satellite position A" should be the more Easterly located in a pair of orbital locations. For up to 4 satellites (preferably numbered from 1 to 4 in a Westwards order), SW 0 may be used. Then, numbers 1 and 3 should use the "Satellite A" position and numbers 1 and 2 the "Switch Option A" position.

5.3. Local Oscillator Frequency

For LNBs (and "intelligent" Switchers) with a single L.O. frequency, and for the High frequency of a switchable pair, the frequency is indicated by connecting one or more diodes from the "Strobe_D" pin (cathode connection) to the "Select" pins (S0 to S3). The diode connections for version 1.0 of the DiSEqC™ Slave software are listed in Table 2. If the frequency is not one of those listed, then the diode for "Not known" should be used. The final two columns in the table indicate the reply sent by version 1.0 software to commands '51h' to '53h' (table list number) and '50h' (frequency string), as defined in Section 6.5. The reply 'E5h' indicates that data is not available and 'E4h' indicates that the requested data follows. Note that the software also returns data values for list numbers which have not yet been defined, so frequencies can be added to the Bus Specification table in the future without the need for changes in the software. These new frequencies would not, of course, be supported by their BCD String values.

5.4. Second Local Oscillator Frequency

For the Low L.O. Frequency of a switchable pair, the same table, Table 2, is employed, but the matrix diode(s) are installed between the Low/High committed output pin (cathodes) and the "Select" pins, S0 to S3. Thus, when

the Low frequency is selected by the DiSEqC™ Slave, the data for the frequency is applied to the selected input pins (S0 - S3).

List number	Diode from Strobe D, or Hi/Lo pin to:				Local Oscillator Frequency	L.O. offset	Response to: 'List number' command	Response to 'BCD String' command:
	S3	S2	S1	S0				
0					None (switcher)		E5	E5
1				✓	Not known		E4 01	E5
2			✓		9.750 GHz	Low	E4 02	E5
3			✓	✓	10.000 GHz	Low	E4 03	E5
4		✓			10.600 GHz	Low	E4 04	E5
5		✓		✓	10.750 GHz	Low	E4 05	E5
6		✓	✓		11.000 GHz	Low	E4 06	E5
7		✓	✓	✓	11.250 GHz	Low	E4 07	E5
8	✓				11.475 GHz	Low	E4 08	E5
9	✓			✓	20.250 GHz	Low	E4 09	E5
10	✓		✓		5.150 GHz		E4 0A	E5
11	✓		✓	✓	1.585 GHz		E4 0B	E5
12	✓	✓			13.850 GHz	High	E4 0C	E5
13	✓	✓		✓	Not allocated		E4 0D	E5
14	✓	✓	✓		Not allocated		E4 0E	E5
15	✓	✓	✓	✓	Not allocated		E4 0F	E5

Table 2: Local Oscillator Frequency signalling

5.5. Slave Family and Peripheral Characteristics

Other characteristics of the Slave's peripheral hardware and facilities are signalled to the DiSEqC™ software by diodes connected between the "Strobe_E" pin (cathodes) and the "Select" pins, S0 to S3. The Slave's address and operational characteristics are determined by diodes connected as in Tables 3 and 4. The (family) address listed in Table 3 is described in Section 6.2.

Diodes connected between Strobe_E and inputs S0 and S1 are used in conjunction to indicate the Slave's "family" characteristics and relevant Bus-address. These generalised family pin allocations were originally intended to define widely differing applications such as combined Positioner / Polariser

(using PWM output) or Dual-Bus controlled switchers. However, the reduced code-size version 1.0 software does not support these more elaborate applications, so the family selection has been adapted to provide more subtle optimization for LNB / Switcher / SMATV usage. The characteristics of these sub-families are indicated in italics throughout this specification because it may not be possible to retain them in future versions of the Slave microcontroller.

Diode from Strobe_E to:				Valid L.O. frequency defined	At least one Committed output used	Slave Type	Address in v1.0
S2	S1	S0	OP5				
				✓	✓	Normal LNB	11h
✓				✓	✓	LNB with Loop-through	12h
					✓	Switcher (d.c. blocking)	14h
✓					✓	Switcher with d.c. loop-through	15h
					see *Table 4*	SMATV	18h +
		✓				Dual-Bus LNB or Switcher	N/A
	✓					Polariser only	21h
	✓		✓			Positioner	N/A
	✓	✓				Installation aid	41h

Table 3a: Address Selection

In version 1.0 software, diodes between Strobe_E and inputs S2 and S3 are used independently to signal whether the Slave application has a “loop-through” capability, and for swapping the pins controlled by the 22 kHz tone in “backwards-compatible” mode (*See section 7.1.*). The loop-through status is available for interrogation in the “Configuration” register by the DiSEqC™ Master via the Bus (*See Table 14*) and also increments the Slave’s address by 1, as shown in *Table 3a*.

Diode from Strobe_E to S3	Diode from Strobe_E to S2	Slave’s Characteristics
		“Backwards compatible” tone drives Hi / Lo pin
✓		“Backwards compatible” tone drives SB / SA pin
	✓	Slave has loop-through facility

Table 3b: Peripheral signalling

If all 4 of the Committed outputs are marked as “not available” (by linking to ground), then the Slave assumes the SMATV address ‘18h’. In version 1.0 software (but not guaranteed for future versions) it is also possible to signal higher address numbers by replacing one or more of the ground-links by a diode to Strobe_E, as shown in *Table 4*.

Link to ground, or Diode to Strobe_E , on pin:				**Slave’s Address**
OP 4	**OP 3**	**OP 2**	**OP 1**	
Link	Link	Link	Link	18h
Link	*Link*	*Link*	*Diode*	*19h*
Link	*Link*	*Diode*	*Link*	*1Ah*
Link	*Link*	*Diode*	*Diode*	*1Bh*
Link	*Diode*	*Link*	*Link*	*1Ch*
Link	*Diode*	*Link*	*Diode*	*1Dh*
Link	*Diode*	*Diode*	*Link*	*1Eh*
Link	*Diode*	*Diode*	*Diode*	*1Fh*

Table 4: SMATV addresses

5.6. Decoded (De-multiplexed) Outputs

In addition to providing encoded (or “multiplexed”) switching outputs (i.e. each switching control output operates independently of the others), the 8 output lines may be used to decode (or de-multiplex) 3 adjacent Committed or Uncommitted switching control lines (e.g. L.O. Frequency, Polarisation and Satellite Position). In this mode just one of the 8 output lines (numbered from OP 1 to OP 8) is active, i.e. “true”, and the other 7 are “false”. The use of a decoded mode is signalled to the Slave software by connecting a diode from the Strobe_E pin (cathode) to either OP 7 (for the Uncommitted group) or OP 8 (for the Committed group), as defined in *Table 5a*.

The single output is normally “Active Low”, but the operation may be changed to “Active High” by adding a diode between Strobe_E and OP 6. Note, however, that during a “hardware reset” the microcontroller always drives all of these pins to the high state.

It is also possible to decode other groups of 3 lines (e.g. Polarisation, Satellite Position B/A and Option B/A) by adding a diode from Strobe_E to OP 5. These alternative decoding formats are defined as Modes 1 through to 8 as shown in *Figure 1* and *Table 5a*.

In version 1.0 software, the ‘OPX’ output is allocated to carry the fourth switching line of the selected group (committed or uncommitted). If not used, this pin should be grounded to ensure that the correct “resources” are reported.

Note that these decoding facilities are purely a “local” characteristic of the Slave, and the available “resources” that are reported over the Bus are the actual switching functions available (e.g. L.O. Frequency, Polarisation and Satellite Position B/A).

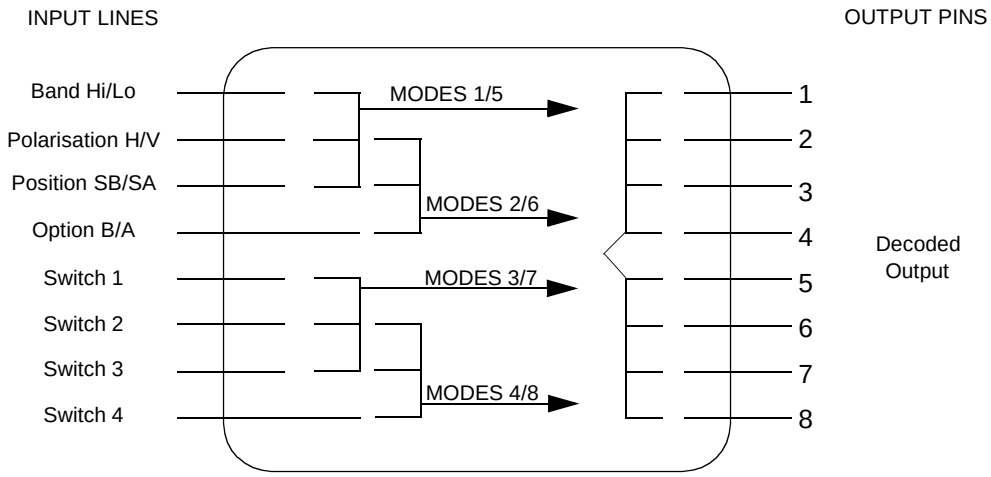


Figure 1 : Scheme of the Decoding Modes

Diode from Strobe_E to OP 8:	Diode from Strobe_E to OP 7:	Diode from Strobe_E to OP 6:	Diode from Strobe_E to OP 5:	Output Port Group	Mode number	Table number	Active Output Polarity
✓				Committed	1	5b	LOW
✓			✓	Committed	2	5c	LOW
	✓			Uncommitted	3	5d	LOW
	✓		✓	Uncommitted	4	5e	LOW
✓		✓		Committed	5	5b	HIGH
✓		✓	✓	Committed	6	5c	HIGH
	✓	✓		Uncommitted	7	5d	HIGH
	✓	✓	✓	Uncommitted	8	5e	HIGH

Table 5a: Decoded Outputs Selection

"Switch Number"	"Satellite Number"	Satellite Position	Polarisation Selected	L.O. Frequency Selected	Active Output Pin	DIL pin number
1	1	A	Vertical	Low	OP 1	5
2	1	A	Vertical	High	OP 2	4
3	1	A	Horizontal	Low	OP 3	3
4	1	A	Horizontal	High	OP 4	2
5	2	B	Vertical	Low	OP 5	1
6	2	B	Vertical	High	OP 6	23
7	2	B	Horizontal	Low	OP 7	22
8	2	B	Horizontal	High	OP 8	21

Table 5b: Decoded Committed Outputs mode (low group) [Modes 1 & 5]

"Switch Number"	"Satellite Number"	Option Switch	Satellite Position	Polarisation Selected	Active Output Pin	DIL pin number
2	1	A	A	Vertical	OP 1	5
4	1	A	A	Horizontal	OP 2	4
6	2	A	B	Vertical	OP 3	3
8	2	A	B	Horizontal	OP 4	2
10	3	B	A	Vertical	OP 5	1
12	3	B	A	Horizontal	OP 6	23
14	4	B	B	Vertical	OP 7	22
16	4	B	B	Horizontal	OP 8	21

Table 5c: Decoded Committed Outputs mode (high group) [Modes 2 & 6]

"SMATV Input"	Switch 3 selection	Switch 2 selection	Switch 1 selection	Active Output Pin	DIL pin number
1	Input A	Input A	Input A	OP 1	5
2	Input A	Input A	Input B	OP 2	4
3	Input A	Input B	Input A	OP 3	3
4	Input A	Input B	Input B	OP 4	2
5	Input B	Input A	Input A	OP 5	1
6	Input B	Input A	Input B	OP 6	23
7	Input B	Input B	Input A	OP 7	22
8	Input B	Input B	Input B	OP 8	21

Table 5d: Decoded Uncommitted Outputs mode (low group) [Modes 3 & 7]

"SMATV Input"	Switch 4 selection	Switch 3 selection	Switch 2 selection	Active Output Pin	DIL pin number
2	Input A	Input A	Input A	OP 1	5
4	Input A	Input A	Input B	OP 2	4
6	Input A	Input B	Input A	OP 3	3
8	Input A	Input B	Input B	OP 4	2
10	Input B	Input A	Input A	OP 5	1
12	Input B	Input A	Input B	OP 6	23
14	Input B	Input B	Input A	OP 7	22
16	Input B	Input B	Input B	OP 8	21

Table 5e: Decoded Uncommitted Outputs mode (high group) [Modes 4 & 8]

If all 8 outputs are not used, then the equivalent (internal) switching line is marked as being "not available" by connecting a diode from Strobe_E to OP 1, OP 2 and/or OP 3, as indicated in *Table 5f*. There is no facility for defining other than 8, 4, 2 or 1 outputs in use, nor reporting "non-default" states back to the Master via the Bus.

Diode from Strobe_E to:			**Active Decoding Outputs:**							
OP 3	OP 2	OP 1	OP 1	OP 2	OP 3	OP 4	OP 5	OP 6	OP 7	OP 8
			✓	✓	✓	✓	✓	✓	✓	✓
		✓	✓		✓		✓		✓	
	✓		✓	✓			✓	✓		
✓			✓	✓	✓	✓				
	✓	✓	✓				✓			
✓	✓		✓	✓						
✓		✓	✓		✓					
✓	✓	✓	✓							

Table 5f: Signalling of Unused Decoding outputs

5.7. "Standard" Configurations

To reduce the number of peripheral components (diodes) required in some common applications, certain hard-wired input combinations (links to ground from the selection pins, S0 - S3), are defined. Since the number of permutations which can be signalled to the selection pins is much reduced, this method can be used only to fully define certain "standard" requirements. Note that the "standard" configuration may be used even if only one L.O.

frequency is implemented, provided that the Hi/Lo pin is correctly strapped to indicate the relevant frequency.

Only one configuration is formally included in version 1.0 software, as given in *Table 6*. This has pins S3 and S2 not-grounded so that it is still possible to signal the "Swap" and "Loop-through" functions with diodes. With version 1.0 software it is valid to tie these pins directly to ground, (instead of via a diode to Strobe E), but there is no guarantee that these configurations (shown in italics) will be retained in future versions of the Slave microcontroller.

The standard configuration with all four pins grounded has been temporarily retained for compatibility with the version 0.1 specification, but this also is not guaranteed to be retained in future versions, so should not be used in new designs.

Pin S3 linked to Vss	Pin S2 linked to Vss	Pin S1 linked to Vss	Pin S0 linked to Vss	Local Oscillator Frequencies, (Lo) + (Hi) GHz	Address (family)	Swap tone function	Loop through
		✓		9.75 + 10.6	11h	No	No
		✓	✓	*9.75 + 10.6*	*11h*	*No*	*No*
	✓	✓		*9.75 + 10.6*	*12h*	*No*	*Yes*
	✓	✓	✓	*9.75 + 10.6*	*12h*	*No*	*Yes*
✓		✓		*9.75 + 10.6*	*11h*	*Yes*	*No*
✓		✓	✓	*9.75 + 10.6*	*11h*	*Yes*	*No*

Table 6: "Standard" Configurations

5.8. Complementary Committed Outputs

Although the standard Slave hardware had a configuration "family" reserved for dual-bus applications (a diode from Strobe_E to pin S0), dual-bus support is not implemented in version 1.0 software. Therefore, if this family is selected, the (Committed) switching outputs normally allocated to the second bus carry instead the complements of the normal Committed outputs. These lines thus carry signals defined as Lo/Hi, V/H, SA/SB and SW0 A/B, which may be of value in circuits where alternate inputs are selected by simple electronic gates, such as diodes. Note that these lines are <u>not</u> tested to identify available "resources", and that this feature is specific to version 1.0 software so may not be retained in future versions.

6. DiSEqCä Bus Commands

The format of DiSEqC™ Data bits and messages is defined in the DiSEqC™ Bus Functional Specification Version 4.2. In principle, a '0' data bit is represented by a 1 ms burst of 22 kHz tone, followed by a 0.5 ms pause, and a '1' data bit is represented by a 0.5 ms tone burst followed by a 1 ms pause. The bits are arranged in groups of 9, the first 8 represent a byte and the final bit completes odd parity for the group. Each byte is transmitted with the most significant bit first and the least significant last.

Version 1.0 software responds to appropriate DiSEqC™ command strings of 3 or 4 bytes, each byte with a following odd parity bit. The first byte carries the DiSEqC™ Framing pattern and some high-level control. The second byte contains the address for one or more Slaves, and the third byte contains a DiSEqC™ Command. Some Commands are followed by one or more Data bytes, as defined in the Command Table. The end of each command string is detected by a pause in the 22 kHz carrier, of greater than approximately 4 ms.

6.1. Framing Byte

The bytes in Table 7, occurring immediately after a 22 kHz carrier gap of at least 15 ms, are recognised by version 1.0 software as valid DiSEqC™ Framing patterns. This version of the software ignores the state of the "Repeated transmission" flag because it does not respond to any commands which would produce undesirable results if duplicated. If the parity bit is incorrect the command is ignored (and no reply is sent).

Hex Bytes	Binary	Framing byte Function
E0, E8	1110 x000	Command from Master, No reply required, First transmission
E1, E9	1110 x001	Command from Master, No reply required, Repeated transmission
E2, EA	1110 x010	Command from Master, Reply required, First transmission
E3, EB	1110 x011	Command from Master, Reply required, Repeated transmission

Table 7: Framing Bytes

6.2. Address Byte (Family + Sub-type)

The DiSEqC™ Slave only acts upon, or acknowledges, command strings which contain an address byte corresponding to the address of the Slave Device. The address byte is divided into two nibbles (4 bits each), the high-nibble "Family" and the low-nibble "Sub-type". Either, or both, of these nibbles may be transmitted (by the Master) as a '0h' ('0000' binary) to indicate a "don't care", or "wildcard". In this case a Slave with any value in the corresponding address nibble(s) responds. If the parity bit is incorrect the command is ignored (and no reply is sent).

6.3. DiSEqCä Command Bytes

Version 1.0 software responds to the indicated commands in *Table 8*. The first column shows which addresses the software accepts as valid for the command, and if blank indicates that the command is not supported. If the address is not valid, or the command is not supported, then a reply 'E5h' is sent. A more detailed description of the commands is given in the DiSEqC™ Bus Functional Specification Version 4.2. If the parity bit is incorrect, the command is not executed but an error reply 'E6h' is sent. If the "Contention" flag does not match the state conditionally specified in certain commands then no reply is sent (to avoid reply collisions).

Valid addresses in v1.0	Hex Byte	Command Name	Command Function	Rec-eived Bytes	Reply Data byte(s)
1x, 21, 41	00	Reset	Reset DiSEqC™ microcontroller	3	
1x, 21, 41	01	Clr Reset	Clear the "Reset" flag	3	
1x, 21, 41	02	Standby	Switch peripheral power supply off	3	
1x, 21, 41	03	Power on	Switch peripheral power supply on	3	
1x, 21, 41	04	Set Cont.	Set Contention flag	3	
1x, 21, 41	05	Contend	Return address **only if** Contention flag is set	3	Address
1x, 21, 41	06	Clr. Cont.	Clear Contention flag	3	
1x, 21, 41	07	Address	Return address **unless** Contention flag is set	3	Address
1x, 21, 41	08	Move C	Change address only if Contention flag is set	4	
1x, 21, 41	09	Move	Change address **unless** Contention flag is set	4	
	0F		Reserved		

Table 8: Command Bytes

Valid addresses in v1.0	Hex Byte	Command Name	Command Function	Rec-eived Bytes	Reply Data byte(s)
1x, 21, 41	10	Status	Read status register (flags)	3	Status
1x, 21, 41	11	Config	Read Configuration (peripheral hardware)	3	Config.
1x	14	Group 0	Read switching state (Committed port)	3	Format
1x	15	Group 1	Read switching state (Uncommitted port)	3	Format
1x	20	Set Lo	Select the Low Local Oscillator frequency	3	
1x	21	Set VR	Select Vertical Polarisation (or Right circular)	3	
1x	22	Set Pos A	Select Satellite Position A	3	
1x, 21, 41	23	Set S0 A	Select Switch Option A (e.g. Linear Pol.)	3	
1x	24	Set Hi	Select the High Local Oscillator frequency	3	
1x	25	Set HL	Select Horizontal Polarisation (or Left circular)	3	
1x	26	Set Pos B	Select Satellite Position B	3	
1x, 21, 41	27	Set S0 B	Select Switch Option B (e.g. Circular Pol.)	3	
1x	28	Set S1 A	Select switch S1 input A (deselect input B)	3	
1x	29	Set S2 A	Select switch S2 input A (deselect input B)	3	
1x	2A	Set S3 A	Select switch S3 input A (deselect input B)	3	
1x	2B	Set S4 A	Select switch S4 input A (deselect input B)	3	
1x	2C	Set S1 B	Select switch S1 input B (deselect input A)	3	
1x	2D	Set S2 B	Select switch S2 input B (deselect input A)	3	
1x	2E	Set S3 B	Select switch S3 input B (deselect input A)	3	
1x	2F	Set S4 B	Select switch S4 input B (deselect input A)	3	
-	30	Sleep	Ignore commands except ‘Awake’ & ‘Reset’	3	
-	31	Awake	Respond to future bus commands normally	3	
1x	38	Write N0	Write to Port Group 0 (Committed switches)	4	
1x	39	Write N1	Write to Port Group 1 (Uncommitted switches)	4	
1x, 21, 41	40	Read A0	Read Analogue value A0	3	byte value
-	41	Read A1	Read Analogue value A1	3	byte value
1x, 21, 41	48	Write A0	Write Analogue value A0	4	
-	49	Write A1	Write Analogue value A1	4	

Table 8: Command Bytes (continued)

Valid addresses in v1.0	Hex Byte	Command Name	Command Function	Rec-eived Bytes	Reply Data byte(s)
-	50	LO string	Read current frequency (BCD string)	3	BCD bytes
1x	51	LO	Read current frequency table entry number	3	F number
1x	52	LO Lo	Read Lo frequency table entry number	3	F number
1x	53	LO Hi	Read Hi frequency table entry number	3	F number
-	58	Write Freq.	Write channel frequency (BCD string)	6	
-	59	Ch. No.	Write (receiver's) selected channel number	5	
-	60	Halt	Stop Positioner movement	3	
-	61		Reserved		
-	62		Reserved		
-	63	Limits off	Disable Limits		
-	64	P Status	Read Positioner Status register	3	Pos. Stat.
-	65		Reserved		
-	66	Limit E	Set East Limit (& Enable recommended)	3	
-	67	Limit W	Set West Limit (& Enable recommended)	3	
-	68	Drive East	Drive Positioner motor East (optional timeout)	4	
-	69	Drive West	Drive Positioner motor West (optional timeout)	4	
-	6A	Store nn	Store Satellite Position & Enable Limits	4	
-	6B	Goto nn	Drive motor to Satellite Position nn	4	
-	6C		Reserved		
-	6D		Reserved		
-	6E	Goto x.x	Drive Motor to angular Position	5	
-	6F	Set Posns.	(Re-) Calculate satellite positions	(4) / 6	

Table 8: Command Bytes (continued)

6.4. Data Bytes

Where the DiSEqC™ Command string consists of more than 3 bytes, then the subsequent bytes are treated as data as defined by the command (as listed in *Table 8*). If any parity bit is incorrect, the command is not executed but an error reply 'E6h' is sent. If an incorrect number of bytes for the relevant command is received, then an error reply 'E7h' is sent.

6.5. Reply bytes

The Slave generates a Reply only if requested by the flag in a valid Framing byte from the Master, and the Address byte (with valid parity) corresponds to that of the Slave. The reply is normally a single byte, as defined by Table 9, except when required by the nature of the Command (listed in the final column of *Table 8*), where additional Data bytes are attached, as defined in *section 8*.

Hex Byte	Binary	Framing byte Function
E4	1110 0100	Reply from Slave, O.K. no errors detected
E5	1110 0101	Reply from Slave, Command not supported by Slave
E6	1110 0110	Reply from Slave, Parity Error detected - Request repeat
E7	1110 0111	Reply from Slave, Command not recognised - Request repeat

Table 9: Reply Bytes

The three types of error report can prevent unnecessary repetitions of commands on the Bus: If the Slave recognises a command as not being supported in its version of software, or by the peripheral hardware, then the ‘E5h’ reply can prevent the Master needlessly repeating it. Reply ‘E6h’ is used if an error is found in Parity or subsequent data, and ‘E7h’ if the command is incorrect (e.g. the wrong number of complete bytes received).

If the Master requests a reply whilst the Reset flag (STATUS.0) remains set (see Section 8.1), then the Slave monitors the Bus and responds after a random delay of between 15 ms and 115 ms, only if no other response is detected. This minimises bus-conflicts if two or more Slaves with the same requested address are present on the Bus during the initialisation process. If a Slave detects another response on the Bus, then the Slave which “lost” the arbitration sets its “Contention” flag and does not reply. Once the Contention flag is set, whenever the Slave receives a command it waits for a period slightly longer than the maximum random delay (but less than 150 ms), and replies only if no other response is detected on the Bus. After the Reset flag is cleared by command ‘01h’ from the Master, then the delay before the reply is fixed at approximately 10 ms (provided that the Contention flag is not set).

6.6. Summary of Error-handling

The Slave does not send a reply if any of the following apply:

The Framing byte is not a valid header from the Master

The Address byte is not appropriate to the Slave's address

There is a parity error in the Framing or Address bytes

The "reply" bit within the Framing byte is not set

The "Contention" flag does not match the conditional state specified in certain commands

The Slave sends an error report byte 'E5h' if:

The Command byte is not recognised as a valid DiSEqC™ command

The particular version of the Slave software does not support the command

The Slave software has detected that a certain command cannot be performed (e.g. standby pin is tied low)

The Slave sends an error report 'E6h' if:

The parity of the Command byte, or any subsequent data bytes, is incorrect

The Slave sends an error report 'E7h' if:

The command message contains the wrong number of (complete) bytes (too many or too few) for the command

If none of the above apply, then the Slave sends the "OK" response 'E4h' and attempts to execute the command. It does not check that individual port switches are controllable, which can be read by the Master software either before or after the command, if verification is required.

7. Control of Output Pins.

When power is applied to the DiSEqC™ Slave microcontroller, or after a Reset command is issued, the software sets all the output pins to defined "Default" levels. Note that during the actual period when a hardware Reset pulse is applied, the microcontroller hardware releases all pins to 'High'. Until a recognisable DiSEqC™ command is detected (i.e. one to which a reply would be sent, if requested), the software operates in "Backwards-compatible" mode and switches the Hi/Lo, H/V and SB/SA pins under the control of the established tone and voltage switch-signalling methods. Once a recognisable DiSEqC™ command is received, any subsequent backwards-compatible signals are ignored. Thus, they may still be sent over the bus (between DiSEqC™ messages) to control an old device such as a "looped through" LNB. In version 1.0 software, the current state of the backwards-compatible pins is not reset when the first DiSEqC™ command is received (so it is possible for the Master to determine whether a Slave has been responding to backwards-compatible signalling).

7.1. Backwards Compatibility

After software initialisation, the Standby pin is taken low (i.e. Power On) to ensure that the external hardware is operational in an environment where there may not be any DiSEqC™ commands. The transmit pin, DTX, is taken low to avoid unnecessary power consumption. The "Switching Option" and "Uncommitted Switches" outputs, SW 0 - SW 4 (or their internal "images" if the decoding facility is in use) are driven low (i.e. to position A), and the three "Committed" outputs take up states determined by the "Backwards-compatible" conditions, as follows:

If the voltage-detection pin, IPX, is pulled low (i.e. indicating that the Bus voltage is nominally below 15 volts), then the H/V pin is driven low to select Vertical Polarisation. Otherwise it is released to high for Horizontal Polarisation.

If a continuous 22 kHz tone is detected (for longer than about 50 ms) then either the Hi/Lo or the SB/SA pin is taken high. The normal function is for the Hi/Lo pin to be driven (to select the high Local Oscillator frequency). However, if a diode is present between Strobe_E and S3 (see Table 4), then the function is swapped so that the SB/SA pin is driven to select Satellite B. When the tone has ceased for approximately 50 ms, the relevant pin is driven low, to select the Low L.O. frequency or Satellite A.

The remaining (allocated) Committed pin (i.e. SB/SA or Hi/Lo) is initially low, but if a DiSEqC™- modulated "ToneBurst" of approximately 13 ms

duration is detected (e.g. a DiSEqC™ byte 'FFh' - but not one starting with the "Framing" nibble 'Eh'), then the pin is switched high. If an unmodulated ToneBurst of similar duration is detected, then the same pin is driven low again. The tolerances for generating these ToneBursts are defined in the DiSEqC™ Bus Specification, versions 3.2 onwards. The Slave microcontroller software responds to modulated bursts of from about 7 to 20 bits, and a continuous ToneBurst of from about 10 to 30 ms.

7.2. "Committed" Control Pins

Function	DIL pin number	PLCC pin number	Pin level	Default	DiSEqCä Command	Write command (38h) data
Low L.O. frequency	5	6	'0'	Yes	20 h	xxx1 xxx0 b
Vertical polarisation	4	4	'0'	Yes	21 h	xx1x xx0x b
Satellite position A	3	3	'0'	Yes	22 h	x1xx x0xx b
Option Switch position 'A'	2	2	'0'	Yes	23 h	1xxx 0xxx b
High L.O. frequency	5	6	'1'	No	24 h	xxxx xxx1 b
Horizontal polarisation	4	4	'1'	No	25 h	xxxx xx1x b
Satellite position B	3	3	'1'	No	26 h	xxxx x1xx b
Option Switch position 'B'	2	2	'1'	No	27 h	xxxx 1xxx b

Table 10: Committed Switching Functions

These pins have functions specifically allocated to existing requirements for the selection of satellite signals, i.e. Horizontal or Vertical plane of Polarisation, High or Low Local Oscillator Frequency and one from a pair of satellites. A further pin has been allocated as an "Options" switch (for example selecting up to two additional satellite positions, or switching between Linear and Circular Polarisation), and may be given a more specific definition in the future. The pins have low nominal default levels, and are controlled by Bus commands, as defined in *Table 10*. If a diode is connected from any pin to the "Strobe_E" pin, as described in *section 5.2.*, then the default and corresponding pin level is set high.

7.3. "Uncommitted" Control Pins

These pins do not yet have specific functions allocated to them. The pins have low default levels and are controlled by Bus commands as defined in *Table 11*.

Function	DIL pin number	PLCC pin number	Pin level	Default	DiSEqCä Command	Write command (39 h) data byte
Switch 1, position A	1	1	'0'	Yes	28 h	xxx1 xxx0 b
Switch 2, position A	23	27	'0'	Yes	29 h	xx1x xx0x b
Switch 3, position A	22	26	'0'	Yes	2A h	x1xx x0xx b
Switch 4, position A	21	25	'0'	Yes	2B h	1xxx 0xxx b
Switch 1, position B	1	1	'1'	No	2C h	xxxx xxx1 b
Switch 2, position B	23	27	'1'	No	2D h	xxxx xx1x b
Switch 3, position B	22	26	'1'	No	2E h	xxxx x1xx b
Switch 4, position B	21	25	'1'	No	2F h	xxxx 1xxx b

Table 11: Uncommitted Switching Functions

7.4. Port-Group Commands

In addition to the commands above which set or clear individual switch states, there are commands to control groups of 4 switching lines. Command '38h' updates the four Committed outputs and command '39h' the four Uncommitted outputs. The new switching combination is defined by a single data byte following the Command byte and is arranged such that any combination of individual switches can be either changed or left in their previous state. This is achieved by allowing the two separate nibbles of the data byte to determine the switches' state in different ways. Any bits set in the high nibble CLEAR the corresponding switch control lines and any bits set in the low nibble SET the corresponding lines. To ensure predictable operation, the high nibble is always applied first, followed immediately by the low nibble. Note this action sequence is purely internal, and the actual pin outputs switch in a single event.

The truth table for the Least Significant Bit (e.g. the L.O. Frequency of the Committed outputs) is shown in *Table 12*, where x does not affect the final state of the L.S.B., so may be either the value 0 or 1. The truth table for the other bits operates in the same way.

Initial Switch Outputs	Command Data Byte	Subsequent Switch Outputs
x x x 0	xxx0 xxx0	x x x 0
x x x 1	xxx0 xxx0	x x x 1
x x x x	xxx1 xxx0	x x x 0
x x x x	xxxx xxx1	x x x 1

Table 12: Truth table for writing to LSB output

7.5. Power Control (Standby) Function

The Power Control output pin is low (‘0’) when the peripheral circuit controlled by the Slave is required to be active, so the pin name “Standby” defines the high (‘1’) output level. Immediately after the Slave is reset, the Standby pin is high, but for backwards compatibility the Slave must power-up without any DiSEqC™ commands being issued. The Standby pin is therefore deactivated a short time after power is applied. Future versions of Slave may default to the Standby mode (to permit multiple Slaves on the Bus without overloading the power supply) so it is recommended that Master control software should issue a “Power On” command (and/or interrogate the STATUS.6 flag) to ensure that the required Slave hardware is activated.

7.6. Analogue Outputs

The standard DiSEqC™ Slave hardware configuration has two “ Analogue” outputs defined, one Pulse Width Modulated (PWM) on output pin ‘OPX’ and one consisting of 8 binary weighted logic outputs, B0 - B7, on the output port pins OP 1 - OP 8. The PWM output might be generated by hardware or completely by software, but neither is available in the “reduced code size” (1 kbyte ROM) version 1.0 of the DiSEqC™ Slave. Therefore, the only method of generating an analogue level is by attaching a digital-analogue converter (in its simplest form just an array of resistors) to some or all of the port outputs OP 1 - OP 8.

Although the “parallel analogue” port, B0 - B7, is treated as an analogue value, it may be used to read (if implemented) and write all 8 output pins (OP 1 - OP 8) in any desired manner, simply by allocating binary weightings to the individual pins.

Since the pin ‘OPX’ is not used for PWM output with version 1.0 software, it has been re-allocated as an extension to the Committed or Uncommitted output port. When the output port is being used in a decoded (demultiplexed) mode, then the ‘OPX’ pin carries the remaining (4 th) control line after the 3 “virtual” lines have been applied to the 3 to 8 line expander. If this pin is not linked to ground, it is reported as an available resource (i.e. up to all 4 lines of either the Committed or Uncommitted port can be reported as controllable, even in the decoding mode). If it is linked to ground then the normal decoder resources are reported over the Bus. In the “Polariser” and “Installer” families, the ‘OPX’ pin may be controlled by the “Switch Option” commands, ‘23h’ and ‘27h’. However, the pin is not tested or reported as an available resource, but the reply ‘E4h’ indicates that the commands are recognised.

8. Status Registers

The Status and related registers provide the means for the DiSEqC™ Bus Master to interrogate the operational conditions of the Slave device. The Slave returns a single data byte (plus an odd parity bit) immediately following the basic “OK” reply header (‘E4h’) to indicate the state of up to 8 defined flags. Unallocated bits are returned as 0, but for compatibility with possible future extensions, this should not be assumed.

8.1. Status Byte

In response to the command ‘10h’, the Slave returns the Status byte, which contains individual flag bits as defined in *Table 13*. The data for flags.2 and .4 is obtained by interrogating the external circuitry as defined in *Table 14*.

Bit Number	Status Function	Implemented in v1.0
.7	Bus-Contention flag is set	Yes
.6	Standby mode has been selected	Yes
.5		Always 0
.4	Auxiliary power is currently available	See Table 14
.3		Always 0
.2	Bus voltage is above nominal 15 volts threshold	See Table 14
.1		Always 0
.0	A Reset has occurred since this flag was last cleared	Yes

Table 13: Status byte

Strobe D pin connected to Vss	“Volts” input (IPX) stored in flag number:	CONFIGURATION.4 flag state
No	STATUS.2	‘0’
Yes	STATUS.4	‘1’

Table 14: Status and Configuration flags detection

8.2. Configuration Byte

In response to the command ‘11h’, the Slave returns the Configuration byte, which contains flags as defined in *Table 15*.

Bit Number	Configuration Function, Device has capability of -	Test condition for Availability	Implemented in v1.0
.7	Analogue output	PWM facility present	Always 0
.6	Standby	'Standby' Not Grounded	Yes
.5	Positioner operation	N/A	Always 0
.4	External Power detection	See Table 14	Yes
.3	Loop-through	Diode from Strobe_E to S2	Yes
.2			Always 0
.1	Signal switching	LNB/switcher/SMATV family	Yes
.0	LO frequency reporting	S0 - S3 input matrix valid	Yes

Table 15: Configuration byte

8.3. Committed Switches Byte

In response to the command '14h', the Slave returns the status of the four Committed output lines. The low nibble of the byte indicates whether the corresponding named signal is controllable and the high nibble indicates its current state. The Committed switching status byte contains flags as given in *Table 16.*

Bit Number	Committed switches state	I/O pin tested	Implemented in v1.0
.7	Options switch position 'B' is selected	SW 0	Yes
.6	Satellite Position B is selected	SB / SA	Yes
.5	Horizontal Polarisation is selected	H / V	Yes
.4	High Local Oscillator is selected	Hi / Lo	Yes
.3	Options Switch is available	SW 0	Yes
.2	Two (or more) satellites are switchable	SB / SA	Yes
.1	Linear Polarisation is switchable	H / V	Yes
.0	Local Oscillator is switchable	Hi / Lo	Yes

Table 16: Committed switches status byte

8.4. Uncommitted Switches Byte

In response to the command '15h', the Slave returns the status of the four Uncommitted output lines. The low nibble of the byte indicates whether the corresponding named switch is controllable and the high nibble indicates its current state. The Committed switching status byte contains flags as given in *Table 17*.

Bit Number	Uncommitted switches state	I/O pin tested	Implemented in v1.0
.7	Uncommitted switch 4 is in position 'B'	SW 4	Yes
.6	Uncommitted switch 3 is in position 'B'	SW 3	Yes
.5	Uncommitted switch 2 is in position 'B'	SW 2	Yes
.4	Uncommitted switch 1 is in position 'B'	SW 1	Yes
.3	Uncommitted switch 4 is available	SW 4	Yes
.2	Uncommitted switch 3 is available	SW 3	Yes
.1	Uncommitted switch 2 is available	SW 2	Yes
.0	Uncommitted switch 1 is available	SW 1	Yes

Table 17: Uncommitted switches status byte

8.5. Positioner Status Byte

The command '64h' requests the Positioner Status byte which contains individual flag bits. However, version 1.0 software does not support positioner functions so the Slave reply is a single byte 'E5h' meaning "not supported".

9. Example Peripheral Circuit

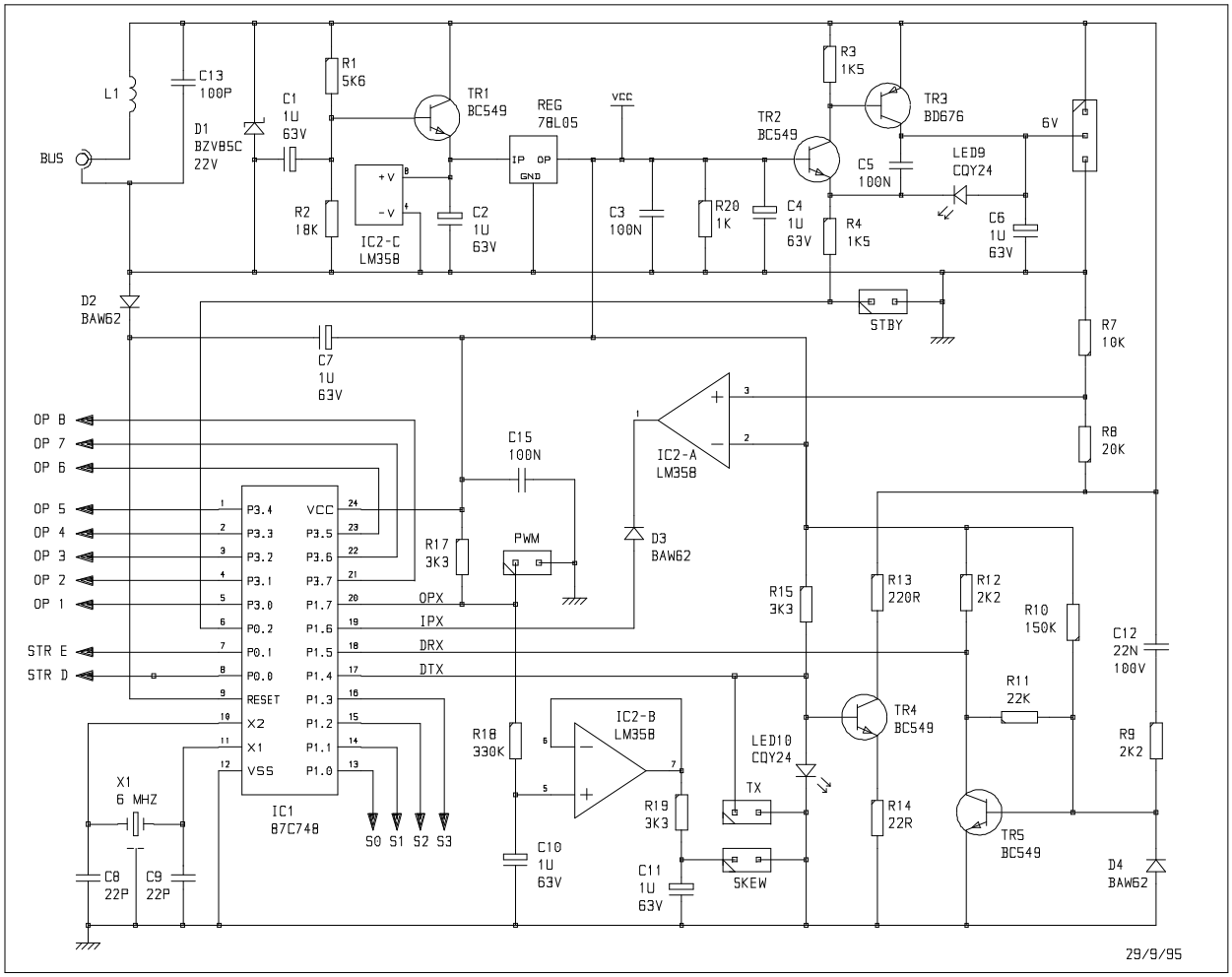


Figure 2 : Example Slave Circuit Diagram

9.1. Circuit Description

Figure 2 shows an example of the Slave peripheral circuitry, implementing most of the normal features. However, it does not include any of the configuration diodes, described in section 5, because of the wide variety of possible locations which they may take. The opportunity has been taken to employ some alternative implementations of standard facilities (e.g. 13/18 volt level detection), but the normal, well established, configurations are equally applicable.

In this implementation, power is derived from the Bus, and a 22 volt zener diode (D1) is included to give some protection against accidental reverse, or excess, voltage application. The power regulator and power supply load capacitances are isolated from the Bus by transistors TR1, 2 and 3, without the need for any inductors.

TR2 and TR3 provide a combined regulation and power-down (Standby) facility, where TR3 may need to be a "darlington" (high gain) device to control currents in excess of about 100 mA. The primary function of LED9 is actually as an offset reference voltage (~ 1.7 volts), with illumination (when active) only as a secondary feature. The peripheral power supply (6 volts in this case) is switched off until the Slave chip, IC1, sinks current (active low) via R4 and TR2. Then TR3 is brought into conduction and the output supply voltage rises until LED9 starts to "steal" TR2's emitter current. At this point the regulator stabilises with about 4.3 volts at the junction of TR2 emitter and LED9 cathode. Although the LED is not a true reference diode, it does have a temperature coefficient similar to that of TR2's base-emitter diode, so thermal stability should be quite good. To regulate to higher output voltages, LED9 could be replaced by a conventional regulator diode. However in this case, a series diode will generally also be necessary to prevent the stage drawing reverse current via the reference diode (when powered-down).

The Bus-data transmitter (TR4) uses LED10 as a reference diode to switch a reasonably stable voltage of about 1 volt across R14, giving a constant-current drive (sink) on to the Bus of about 40 mA. This gives the nominal 650 mV swing across the 15Ω load at the (DiSEqC™ Master) end of the Bus cable.

The Bus signal detector is TR5, which is biased very close to saturation and with a shunt-feedback voltage gain of about 10 (R11 / R9). With a nominal minimum input tone of 150 mV peak (300 mV peak-peak), TR5 collector rises by about 1.5 volts to just reach IC1's input threshold voltage, and begin detection. The substantially virtual earth input impedance of TR5, with the input circuit C12 / R9 time constant of about 50 µs, gives a high-pass filtering characteristic to rapidly remove any low-frequency voltage disturbances on the Bus. A small capacitor (typically 100 pF) from the collector to base of TR5 may be beneficial in reducting the gain at frequencies well above 22 kHz. The DiSEqC™ Slave ic uses (negative-going) edge-triggered internal hardware on the DRX pin to detect the presence of the carrier tone and so may also respond to rapid "spikes" of noise. D4 is included to protect the base-emitter junction of TR5 against possible rapid negative-going voltage steps from the Bus.

For backwards compatibility with 13 / 18 volt switching systems, a voltage detector with a nominal threshold of 15 volts and a tolerance of no more than ± 1 volt is required, i.e. ± 6.7 %. Using a nominal 5 volts regulator tolerance of 4 % - 5 %, and voltage divider resistors of ± 1%, there is no scope for further errors. Therefore, a cheap Operational Amplifier, IC2-A, has been employed to give negligible offset voltage and negligible current loading on the divider resistors R7 and R8. The Op-Amp is operated from a higher

voltage than the 5 volts Vcc of the microprocessor so D3 is included to permit the Op-Amp to pull down the sensing pin (IPX) but not pull it up above Vcc. Note that the Operational Amplifier is a type which can operate with input and output signals very close to the negative supply (ground) potential. The second half of IC2 is used as a buffer to avoid loading the PWM low-pass filter R18 / C10, however the PWM facility is not implemented in the Version 1.0 software.

During normal operation, the Strobe outputs (STR_D and STR_E) float, and the configuration pins (S0 - S3) are weakly pulled high by the current sources internal to the DiSEqC™ chip. When the software needs to determine the external configuration, at power-up or reset, then it pulses low the appropriate Strobe pins in turn. When one or more diodes are present between appropriate pins, then the corresponding inputs are pulled low and detected by the internal software.

Note: Where the Slave is to be powered from the Bus, the reset time can be made less than the required 100 ms by connecting in parallel with the diode D2 (or by replacing it by) a resistor of typically 22 kΩ.